A Switched-Capacitor degenerated, scalable $gm-C$ filter-bank for acoustic front-ends

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***Abstract*—Filter-banks based on a $gm-C$ topology are popular in acoustic sensor systems targeting spectral analysis. Their benefits lie in a very low power consumption and center-frequency scalability through gm-tuning to cover the audio frequency range. However the linear signal swing at the output of the filter is limited due to the inherent non-linearity of the input transistors in a differential pair. This work assesses the impact of noise and center-frequency specifications on the power consumption of 2 OTA based $gm-C$ bandpass filters, both from a theoretical and practical point of view. Next, we introduce a novel scalable switched-capacitor based degeneration technique that enhances the linear signal swing at the filter output. Simulation results in 90nm CMOS demonstrate a power consumption of only $44nW$ for a bandpass filter with Q-factor of 1 with 63 dB dynamic range ($<2\%$ THD) and a center-frequency of $100Hz$. This scales to only $1.4\mu W$ for a center-frequency at $3.2kHz$. These power consumption numbers compare favorably with the state-of-the-art and enhance the Figure of Merit by more than 1.5X for a similar dynamic range.**

I. Introduction

Acoustic processing for power constrained applications such as cochlear-implants or voice activity detection systems, often decompose the audio signal into multiple frequency bins for time-spectral analysis. Such analysis helps to identify patterns in the acoustic spectrum for tasks such as recognition or classification [1], [2]. Analog bandpass filter-banks based on a $gm-C$ topology are commonly used for these applications and typically cover the acoustic frequency range from few tens of Hz to a few kHz. For a low input referred noise, it is desirable to precede these filter-banks by a high gain amplifier and hence these filters need to handle large signal swings without introducing significant distortion. Existing filter-banks use non-standard CMOS transistors such as floating gate devices [1], [3] or require potentials larger than V_{DD} [4] to achieve linearity and gm based center-frequency (f_c) scalability. The commonly used resistor based degeneration technique to improve linearity is not suitable in the acoustic frequency range, as very large resistors ($\sim 100M\Omega$) are needed that incur area penalty for implementation in a CMOS process.

This work theoretically assesses the noise and frequency dependent bounds on the power-consumption of bandpass $gm-C$ filters in Section II, after which Section III introduces a novel switched-capacitor based degeneration technique that enhances the linear signal swing at the filter output and moreover allows for convenient f_c scaling in the filter-banks.

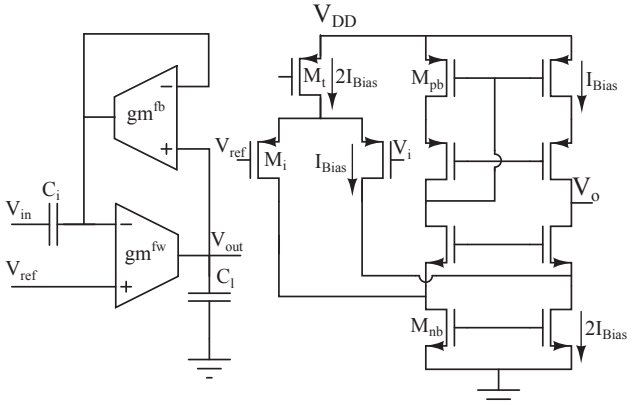

Fig. 1. $gm-C$ filter architecture used in analysis (left) and the folded cascode transconductor (right) used for gm cell implementation

II. Theoretical analysis for power bounds on $gm-C$ filters

$gm-C$ based filter architectures are the most commonly used topology in acoustic filter-bank applications, as they allow very low power operation together with frequency tunability, albeit with a limited linear swing at the transconductor output. Switched-capacitor filters, on the other hand, allow for a wider linear output swing, however at a much larger power consumption than $gm-C$ filters. This power penalty stems from the need for a unity gain bandwidth well beyond the used switching clock frequency. Detailed analysis for frequency and noise specification aware power bound for a 2 OTA based bandpass $gm-C$ filters is presented in this section.

The $gm-C$ filter architecture analyzed for noise and frequency dependent power bound estimation is shown in Fig.1. Although this analysis assumes a folded cascode implementation for the transconductor as shown in Fig. 1, right, it can easily be adapted to other transconductor topologies. The transfer function of BPF in Fig.1 can be written as,

$$\frac{v_{out}}{v_{in}} = \frac{-s\frac{C_{in}}{gm_i^{fb}}}{1+s\frac{C_l}{gm_i^{fw}}+s^2\frac{C_lC_{in}}{gm_i^{fb}gm_i^{fw}}} \quad (1)$$

where the superscripts fb and fw indicate contributions from the feedback and the forward path respectively. Also, the subscript text in the gm corresponds to the transistor naming in the transconductor cell. Comparing the denominator of Eq. 1

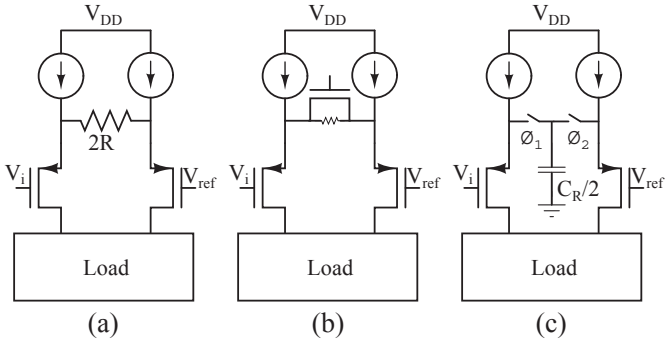

Fig. 2. Traditional resistive (a) and MOSFET in triode (b) based degeneration. Proposed switched-capacitor (c) based degenernation

with the standard second order denominator polynomial shows that the f_c and Q factor are defined by

$$f_c = \frac{1}{2\pi}\sqrt{\frac{gm_i^{fb}}{C_{in}}\frac{gm_i^{fw}}{C_l}} \quad Q = \sqrt{\frac{gm_i^{fw}}{gm_i^{fb}}\frac{C_{in}}{C_l}} \tag{2}$$

The noise current spectral density at the filter output due to noise generated in the forward path can be written as

$$S_{Io}^{fw} = \frac{16}{3}kT(gm_i^{fw} + gm_{nb}^{fw} + gm_{pb}^{fw}) \tag{3}$$

The transistor sizes are assumed to be sufficiently large so that the flicker noise contribution is limited to less than 10% of the total noise contribution and is ignored in the further analysis. The cascode transistors are biased such that their noise contribution is insignificant. Similarly the noise current spectral density at output due to the feedback path can be written as

$$S_{Io}^{fb} = \frac{16}{3}kT(gm_i^{fb} + gm_{nb}^{fb} + gm_{pb}^{fb})\Big(Zin(s)gm_i^{fw}\Big)^2 \tag{4}$$

where $Zin(s) \approx \frac{1}{sCin}||gm_i^{fb}$ is the impedance looking into the inverting node of the forward path. From Eq. 3 and 4 the total noise current density at the output node is

$$S_{Io}^{total} = S_{Io}^{fw} + S_{Io}^{fb} \tag{5}$$

Without loss of generality, further analysis assumes that the same transconductor is used in the forward and the feedback path i.e $gm_x^{fw} = gm_x^{fb} = gm_x$. This allows the total noise current spectral density at the filter output to be expressed as

$$S_{Io}^{total} = \frac{16}{3}kT(gm_i + gm_{nb} + gm_{pb})\Big(1 + (Zin(s)gm_i)^2\Big) \tag{6}$$

For frequencies around f_c, $|Zin(s)| \approx \frac{1}{2gm_i}$ hence the total integrated output noise power over $f_{\pm 3dB}$ can be expressed as

$$v_{no}^2 \approx \frac{20}{3}kT\frac{(gm_i + gm_{nb} + gm_{pb})}{2\pi}\int_{f_{-3dB}}^{f_{3dB}}\left(\frac{1}{fC_l}\right)^2 df \tag{7}$$

$$\approx \frac{20}{3}\left(\frac{kT}{C_l}\right)\frac{gm_i + gm_{nb} + gm_{pb}}{2\pi C_l}\frac{f_{3dB} - f_{-3dB}}{f_{3dB}f_{-3dB}} \tag{8}$$

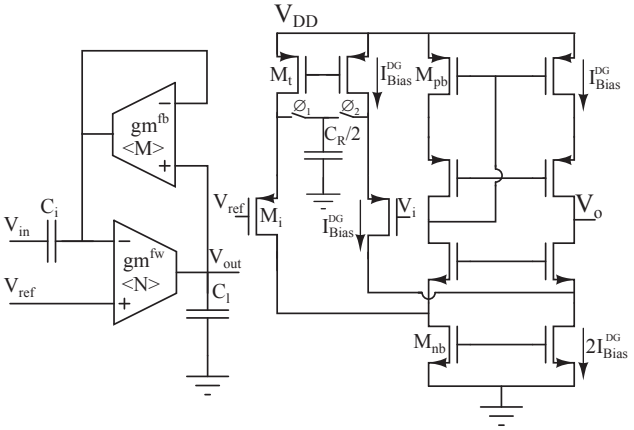

Fig. 3. Switched-capacitor degenerated $gm - C$ filter (left) and the degenerated transconductor implementation (right).M and N indicate the number of parallel cells in the feedback and the forward path respectively

Furthermore, as the bias current through M_i and M_{pb} are identical and about one half of current through M_{nb}, $gm_i + gm_{nb} + gm_{pb}$ will typically range between $3gm_i$ to $4gm_i$. Also, Eq. 8 allows to approximate input referred noise $v_{ni} \approx v_{no}$ in the frequency range of $f_{\pm 3dB}$ as in this frequency range $|v_{out}/v_{in}| \approx 1$. Although this ignores the second order transfer function and omits integration beyond $f_{\pm 3dB}$ range, simulation results in Section IV across the whole $0.1f_{-3dB}$ to $10f_{3dB}$ range will demonstrate a discrepancy of only $\sim 30\%$ due to this approximation. Power bounds can be computed by assuming a $gm/I_{bias} = \alpha$ with Eq. 8

$$v_{no}^2 \approx \frac{20}{3}\left(\frac{kT}{C_l}\right)\frac{I_{bias}(\alpha_i + 2\alpha_{nb} + \alpha_{pb})}{2\pi C_l}\left(\frac{f_{3dB} - f_{-3dB}}{f_{3dB}f_{-3dB}}\right) \tag{9}$$

The output linear range of the filter topology in Fig. 1 is limited by the linearity of the input transistor pair of the forward and the feedback path. Due to unity gain feedback path, the signal swing at the inverting node of the forward path equals the swing of the output signal v_{out}. The maximum swing that the input pair can tolerate is limited to $\sqrt{2}(V_{GS} - V_T)$ for a hard non-linearity. For a 90 nm CMOS technology, and a dc-bias point of $V_{DD}/2 = 600mV$, the maximum signal swing would be limited to less than $100mVpp$ for similar $V_{GS} - V_T$ for transistors M_i and M_t. Hence even though $gm-C$ filters are attractive from the power consumption point of view, the output linear swing is quite limited. The next Section will therefore introduce a novel switched-capacitor based degeneration technique which exactly enhances the linear signal swing at the output of $gm - C$ filters and is also perfectly suitable for standard CMOS implementation.

III. Switched capacitor based degeneration

Resistive degeneration as shown in Fig. 2(a) allows local feedback and reduces the signal swing across the input tran-

TABLE I
TARGET SPECIFICATIONS

num. of channels	f_c range (Hz)	Q factor	Integrated output noise	Output signal swing
6	100 - 3200 Octave spacing	1	$< 100\mu V_{rms}$	$> 400mVpp$ $< 2\%$ THD

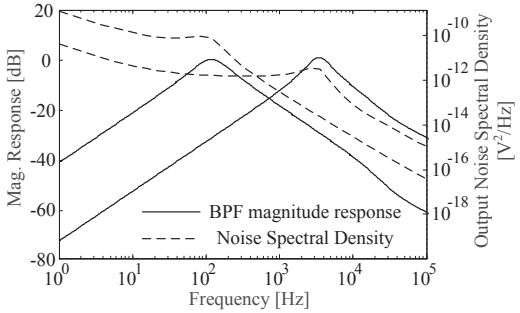

Fig. 4. Simulated magnitude response and output noise voltage spectral density $S_{vo}(f)$ for the switched-capacitor degenerated filter for the first and the last channel in 90nm CMOS

sistors. This allows a wider linear swing at the output. The effective transconductance of a degenerated differential pair is

$$gm_{eff} = \frac{gm_i}{1 + gm_i R} \approx \frac{1}{R} \quad if \quad gm_i R >> 1 \tag{10}$$

For the audio-frequency range, the necessary resistor value for $gm_i R >> 1$ tends to be of the order of $\sim 100M\Omega$ for capacitor value of few tens of pF. Such a resistor is uncomfortably large to be implemented as a resistor in a CMOS process. Moreover, the resistance value is not very well controlled in CMOS processes hence restricting the use for such applications. Degeneration may be also achieved by using transistors in triode region as shown in Fig. 2(b). However, they are of limited use because for larger signal swings, the degenerating transistors are no longer in deep triode region and the value of the induced resistor would vary with the signal amplitude which defeats its purpose.

This work proposes a switched-capacitor based degeneration, as shown in Fig. 2(c). The effective resistance between the two source nodes in Fig. 2(c) can be expressed as $2/(f_s C_R)$. We will demonstrate that such an implementation is extremely linear and allows for f_c and Q-factor scalable filter design by varying the number of parallel g_m cells in the feedback and forward path. Moreover, also at run-time f_c can be fine tuned by varying the f_s or switched-capacitor, C_R, or a combination of both. The effective transconductance can be then expressed from Eq. 10 as

$$gm_{eff} \approx f_s C_R \qquad if \quad (gm_i / f_s C_R) >> 1 \tag{11}$$

The resulting filter topology with the same switched capacitor based degeneration in the forward and the feedback path is shown in Fig. 3. The transfer function for this filter for one gm cell in the forward and the feedback path ($M = N = 1$) can be expressed as

$$\frac{v_{out}}{v_{in}} \approx \frac{-s\frac{C_{in}}{f_s C_R}}{1 + s\frac{C_l}{f_s C_R} + s^2 \frac{C_l C_{in}}{f_s^2 C_R^2}} \tag{12}$$

TABLE II
SIMULATED NOISE AND LINEARITY RESULTS IN $90nm$ CMOS.

f_c (Hz)	Integrated output noise	Output signal swing
100	$87\mu V_{rms}$ $f_{-3dB} < f < f_{+3dB}$ $121\mu V_{rms}$ $0.1f_{-3dB} < f < 10f_{+3dB}$	$510mV_{pp}$; $< 1\%$ THD $800mV_{pp}$; $< 5\%$ THD
3200	$86\mu V_{rms}$ $f_{-3dB} < f < f_{+3dB}$ $116\mu V_{rms}$ $0.1f_{-3dB} < f < 10f_{+3dB}$	$484mV_{pp}$; $< 2\%$ THD $700mV_{pp}$; $< 5\%$ THD

This allows the f_c and Q factor to be defined by a tunable capacitor ratio, being

$$f_c \approx \frac{1}{2\pi}\sqrt{\frac{gm_{eff}^2}{C_l C_{in}}} \approx \frac{f_s}{2\pi}\sqrt{\frac{C_R}{C_{in}}\frac{C_R}{C_l}} \quad Q = \sqrt{\frac{C_{in}}{C_l}} \tag{13}$$

By similar analysis as in Section II, the total output noise current density S_{Io}^{fw} due to the forward path can be written as

$$S_{Io}^{fw} = \frac{16}{3} kT(gm_t^{fw} + gm_{nb}^{fw} + gm_{pb}^{fw}) + 8kTf_s C_R \tag{14}$$

The noise contribution of the input transistors in the degenerated transconductor is not significant, as they effectively appear as cascode devices. Due to splitting of the tail current sources, their noise contribution is no longer common mode and contributes to output noise as in Eq. 14. The last term of Eq. 14 is the noise contribution of the switched-capacitor based degeneration resistor. Following a similar analysis as in Section II the total output noise can hence be estimated as

$$v_{no}^2 \approx \frac{kT}{C_l}\left(\frac{20}{3}\frac{gm_t + gm_{nb} + gm_{pb}}{2\pi C_l} + 10\frac{f_s C_R}{2\pi C_l}\right)\left(\frac{f_{3dB} - f_{-3dB}}{f_{3dB} f_{-3dB}}\right) \tag{15}$$

Similar to Eq. 9, the power consumption can be estimated from I_{bias}^{DG} from the equation below

$$v_{no}^2 \approx \frac{kT}{C_l}\left(\overbrace{\frac{20}{3}\frac{I_{bias}^{DG}(\alpha_t + 2\alpha_{nb} + \alpha_{pb})}{2\pi C_l}}^{\text{dominant}} + \overbrace{10\frac{f_s C_R}{2\pi C_l}}^{\text{non-dominant}}\right)\left(\frac{f_{3dB} - f_{-3dB}}{f_{3dB} f_{-3dB}}\right) \tag{16}$$

From Eq. 16 and 9, it can be seen that, as compared to the non-degenerated transconductor, the noise power in degenerated transconductor is a factor I_{bias}^{DG}/I_{bias} times higher. This excess noise is in addition to a non-dominant noise contributed by the switched capacitor based resistor. This higher noise trades-off with increased linearity, as degeneration transforms the transconductance from a v_{in} dependent non-linear value of gm_i to an independent linear value of $f_s C_R$. Further, as highlighted previously, implementing the degenerating resistor as a switched capacitor allows integrating large resistors for degeneration necessary in the audio frequency range.

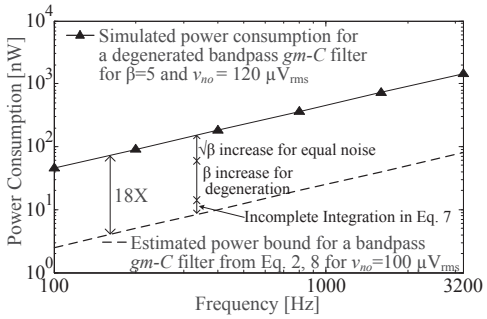

Fig. 5. Comparison of the simulated power consumption of the switched-capacitor degenerated filter in 90 nm CMOS with the theoretical bounds on $gm-C$ filter as computed from Eq. 9 for constant integrated output noise

IV. Filter-bank implementation and Results

This section first details the design procedure for a single BPF and then presents the complete implementation of a 6-channel filter-bank by scaling the f_c. Table I highlights the targeted specifications for the filter-bank to be implemented in a 90 nm CMOS technology.

The gm_{eff} and the minimum C_l necessary to meet the f_c and the noise specifications for the first filter ($f_c = 100Hz$) are estimated from Eq. 13 and 16 to be $gm_{eff} \approx 25nS$ and $C_l \approx 40pF$ for a degeneration factor of $\beta = gm_i/f_sC_R = 5$. For a Q-factor of 1, $C_l = C_{in}$ from Eq. 13. The capacitor values can be further reduced by maximizing the gm/ID for M_i and minimizing for M_t, M_{pb}, M_{nb} respectively. The final values that achieve the required noise and linearity specifications are $C_l = 25pF$ and $gm_{eff} = 16nS$. Though, the implementation here is for a Q-factor of 1, non unity Q-factors may be realized by varying the ratio C_{in}/C_l and/or the number of parallel g_m cells in the forward (N) and the feedback (M) path.

The f_s for switched-capacitor degeneration is chosen to be $512kHz$, which is greater than 100 times the maximum f_c, as this allows the intermodulation distortion to be attenuated by more than 40dB under first order filter-roll off. Moreover, selecting such high f_s allows to use a small $C_R = 20fF$, thus minimizing the area impact.

To use the proposed filters in a complete filter-bank, gm_{eff} is scaled linearly from filter to filter by increasing the number of parallel cells in the forward (N) and the feedback path (M), which scales $f_c \propto \sqrt{MN}$. This allows for a constant integrated output noise independent of f_c. The periodic-ac and the periodic-noise analysis are used to simulate the magnitude response and the output noise voltage spectral density. These results for the first and the last channel of the bandpass filter-bank are shown in Fig. 4. Results of the transient analysis for the maximum linear swing along with the integrated output noise for the first and the last filter are shown in Table II.

Figure. 5 compares the simulated power consumption of the switched-capacitor degenerated $gm-C$ BPF filters with the theoretical limit of regular $gm-C$ bandpass filters as a function of f_c for a fixed integrated output noise. It can be seen from Fig. 5 that the power consumption is $\sim 18X$ larger than the theoretical limit of non-degenerated $gm-C$ topologies. As illustrated in Fig. 5, this can be accounted for by the power penalty incurred due to degeneration (βX), maintaining the same integrated noise as the non-degenerated transconductor ($\sqrt{\beta}X$) and the incomplete integration of noise in Eq. 7.

TABLE III
Comparison with State of the art

Specs.	This work	[3]	[4]	[5]	[1]
Tech.	90 nm	0.8 μm	0.35 μm	1.5 μm BiCMOS	0.35 μm
V_{DD} (V)	1.2	1.25	1.2	2.8	3.3 [1]
DR (dB)	63/66	> 62	62.9	66	61.5
(%) THD	$< 2/< 5$	1	< 1.1	5	0.84
Power (μW)	0.09/0.9	2.5	< 16	0.12/3.36	0.19/2.85
@ freq. (Hz)	200/2k	2 k	100/20k	200/10k	200/2k
$\frac{FoM/1p}{\frac{PowerV_{DD}}{nf_cDR}}$	$\frac{0.19/0.14}{< 2/< 5}$ thd	< 0.62	< 0.34	0.23	1.3

[1] assumed for a 0.35μ CMOS process

Table. III compares the degenerated $gm-C$ filter-bank to the state-of-the-art (SoTA) filter-banks for similar frequency range. It can be seen that the power consumption of this filter-bank compares favorably with the SoTA for a similar dynamic range inspite of the implementation in a sub-100nm technology. This affords a greater than $1.5X$ improvement in the Figure-of-Merit (FoM) proposed in [6]. Also, this design, unlike the SoTA does not need non-standard CMOS transistors such as floating gate devices or BiCMOS technology.

V. Conclusion

This work evaluates the noise and frequency dependent power bounds on 2 OTA based $gm-C$ bandpass filters and proposes a novel alternative switched-capacitor based scalable degeneration technique. The introduced topology allows increasing the linear signal swing at the filter output to $484mV_{pp}, (DR = 63dB)$ and $700mV_{pp}, (DR = 66dB)$ for $< 2\%$ and $< 5\%$ THD respectively for a power supply voltage of $1.2V$ in 90 nm CMOS. The power consumption of the proposed filter-bank compares favorably to SoTA and enhances the FoM by more than 1.5X.

Acknowledgment

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